Amendments to the Specification

Please replace paragraph [0003] of the specification with the following text.

The existing MESI states may possess certain performance-limiting attributes. In one situation, when a modified cache line in ~~a inner-level~~ an inner-level cache (e.g. level 1 cache) wishes to become invalid and write its modified data up to an outer-level cache (e.g. level 2 cache), the outer-level cache may in turn become invalid and write its modified data to an even more outer-level cache or to system memory. This may not be advantageous if there is significant traffic on the outer-level interfaces. In another situation, when a snoop request arrives at ~~a outer-level~~ an outer-level cache, it must be sent down to any inner-level caches. This may not be advantageous if there is significant use of the inner-level caches over the inner-level interfaces.